As discussed further herein, the Office Action fails to recognize that in Cutts the first processor is not free to access any location only in a first memory at any time in order to write data, as recited in the present claims. Similarly, the second processor is not free to write access any location only within a second memory at any time. Instead, unlike the present invention, in Cutts, the processors must await a private write command and that time, both processors must access the same location in their respective memories. Thus, none of the claims can be anticipated by Cutts. Further, in Cutts the processors operate on identical instruction streams and cannot be used to control a system using independent processors, as the Office Action suggests. Thus, the references cannot be combined to render the claims unpatentable.

Present claim 23 recites an apparatus with a first processor, a second processor, a first memory and a second memory. The first processor has write access at any time to any location in the first memory and read access at any time to any location in the first and the second memory. Similarly, the second processor has write access at any time to any location in the second memory and read access to any location in the first and second memory.

The system according to the present invention provides highly responsive data write capability and does not have disadvantages associated with interrupt based or other synchronous systems. For example, in a system according to the invention used to control a laser, it may be useful to respond immediately to overheating conditions. One processor can monitor temperature conditions systemwide and write such data to locations in the first memory as the data are available. The second processor may be dedicated to laser control functions, writing appropriate data to memory locations in the second memory. Each processor operates independently and, according to the invention, can write data to any location in its respective memory at any time. This ability for a processor to write to any

of its memory locations at any time eliminates data write latency and provides powerful advantages over the system disclosed in Cutts alone or in combination with Nagai.

Column 2, lines 26-28 and column 3, line 65 through column 4, line 5 of Cutts disclose an arrangement in which a plurality of processors, 11-13 all execute the same instruction stream except during power up self-test and diagnostic testing. Column 2, lines 28-30 and column 4, lines 5-8 of Cutts disclose that memory number 1, designated 14 in the drawings, and memory number 2, designated 15 in the drawings, store the same data in the same address space. Cutts seeks to achieve loose synchronization by detecting events such as memory references and acting to stall any CPU ahead of other CPUs until all CPUs execute the function simultaneously. In Cutts, the shared memory space also includes a private write area assigned under software control as a private memory in each of the memory modules 14, 15. The private memory area is divided between the three CPUs, so that each area can be written by only one of the CPUs. The CPUs then read each of the locations and compare the data for diagnostic purposes or to detect the cause of an interrupt.

Cutts fails to disclose an arrangement as recited in the present claims in which a processor may write to any memory location in its area at any time. This feature of the present invention allows asynchronous operation of processors. Unlike Cutts, which requires the processors to execute the same instructions at the same time, in the present invention, a processors's ability to write to any memory location in its area at any time allows the processors to execute entirely different and unrelated streams of instructions and to operate asynchronously of each other. This independent operation is simply not possible in Cutts. Indeed, in Cutts a private write command is executed by all processors at the same time. Thus, each processor is not free to write to any location in its memory area at any time, as recited in the present claims.

Moreover, Cutts specifically discloses maintaining synchronous relationships, which the present invention seeks to avoid entirely. Column 32, lines 11-14 discloses that during the private write procedure in Cutts, all three CPUs present the same address on their bus, even though different data may be present. Thus, in contrast to the recitations in the present claims, Cutts fails to disclose a system in which a processor can write to any address in its portion of memory at any time.

The requirement in Cutts for the processors to execute the same sequence of instructions and to present the same address on their bus during a private write command, is entirely at odds with the abilities provided by the invention recited in the present claims. In the present invention, processors are free to execute different streams of instructions and to write to any memory location in their memory areas at will. This ability to perform different sets of tasks in the present invention allows individual processors to be dedicated to performing a specific task and provides a convenient means for exchanging information among processors without latency associated with writing delays. For example, since the second processor can write access the second memory at any time, when the first processor accesses data from the second memory, the first processor is assured access to the latest data available consistent with the second processor's processing steps. This is simply not the case in Cutts, in which each of the processors executes the same sequence of instructions and the same address of the various private memory areas is written at the same time.

There is no suggestion anywhere to combine the references. Nagai merely discloses a system with multiple processors. There is no suggestion of the features recited in the present claims. Cutts fails to disclose a system which provides immediate memory data write access by different processors to different memories, while allowing both processors to read from both memories. Finally, even if the references are combined, one does not arrive at the present invention, because Cutts used with the multiple

processors of Nagai still fails to disclose the ability of a processor to access only its corresponding memory at any time for writing data while accessing either memory for reading data. There is no suggestion in the art to further modify the combination to provide the features recited in the present claims.

In view of the radically different philosophical approaches between the invention recited in the present claims and the disclosure in Cutts, and because Cutts fails to disclose important features recited in the claims, including the ability for a processor to access any location in its area at any time, the present claims are patentably distinguished over Cutts and Nagai, alone or in combination. Early notification of same is earnestly solicited.

Respectfully submitted,

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